A Mixed-Mode Conditioning Circuit Designed for Adaptive Smart Sensing

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Abstract – **This paper explains the design and simulation of a conditioning circuit based on a current-mode mixed analogue-digital adaptive processor. The proposed processor model consists of two main blocks: a D/A four quadrant multiplier and a current conveyor that performs the non-linear output function. Applied to sensors conditioning, the processing system customizes its free parameters, stored in digital registers, adapting the response. System simulation results and achieved performance are presented.**

1 INTRODUCTION

Sensors are the first stage of a data processing system connected to the real world. Usually, its behavior is not linear along the whole sensor working range. Often, this drawback makes necessary to include a pre-processing circuit in the data path which will extend the linear output span, improving the system performance.

In these cases, the use of adaptive processing circuits allows to fit to the behavior of a determined sensor. Moreover, adaptability allows to adjust the circuit operation to changes in sensor response due to aging, environmental effects, or simply sensor replacement, giving the best performance every time.

Artificial Neural Networks (ANNs) are bio-inspired computing tools based on neural system operation [1]. The performed transfer function is learned by means of a training process where input-output data pairs are iteratively presented, adjusting the system free parameters (called weights). Depending on the application requirements, the very restricted set of arithmetic operations performed by these processors make them suitable to be implemented in application-specific circuits. When size, power consumption and speed are main requirements, electronic analogue implementation is a proper selection. Today, shrinking bias voltages makes difficult to processing data in voltage-mode. In this case, current-mode processing gives better results at lower bias, reducing the power consumption [2].

On the other hand, implementation of reliable long-term and mid-term analogue programmable weights results very hard due to mismatching and offsets. Due to the high accuracy of digital storage data for long and mid-term in register-based structures, the combination of both electronic technologies can improve the system features. Previous works [3], [4] have presented the use of mixed-mode multipliers in adaptive processors implementation, showing promising results applied to real problems.

This paper presents the analysis and simulation of a current-mode based artificial neural network with digital weight storage showing its performance in sensor linearization tasks.

The paper is structured as follows: Section 2 presents the architecture of the proposed adaptive processor, building blocks and electronic design. Section 3 presents the circuit simulation results, differences with ideal arithmetic behavior and the mathematical models used in the next section. Section 4 shows two application examples of this processor: linearization of two samples of a negative temperature coefficient resistor and two samples of a giant magneto-resistive sensor. We will present simulation results of both applications. Finally, the conclusions of this work are proposed.

2 PROCESSOR ARCHITECTURE

The processor architecture is shown in Fig. 1. Current-codified data are multiplied by an 8-bit digital value that weights the influence of the corresponding input to the artificial neuron output. Four-quadrant multiplier (ADM in Fig. 1) is based on a NMOS R-2R current ladder architecture, multiplying the input value by an 8-bit number between -1 and +1. After weighted currents are accumulated, final output is given by a non-linear circuit that performs the sigmoid function. Processor blocks have been designed using the Austria Microsystems (AMS) 0.35 μm design kit. In order to achieve limited power consumption, maximum processing currents are restricted to ± 50 μA and maximum voltage bias are limited to 3.3 v.

2.1 Four-quadrant multiplier architecture

The proposed analog-digital multiplier unit (ADM, Fig. 1) is depicted in Fig. 2. This circuit contains a current inverter controlled by the sign bit of the digital operand plus a 7-bit digitally programmable current divider. Current output ranges from I_{in} to $-I_{in}$. An analog multiplexer selects the current input path to the R-2R ladder. When the weight sign bit is

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positive (b_0=0 v), current goes to the divider straight; if sign bit is negative (b_0=3.3 v), current is driven to the inverter, changing the sign of the output current.

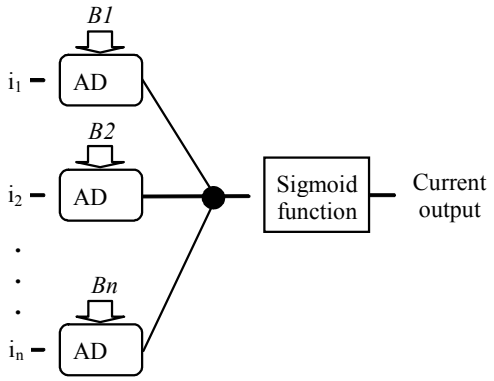

Figure 1: Adaptive processor architecture

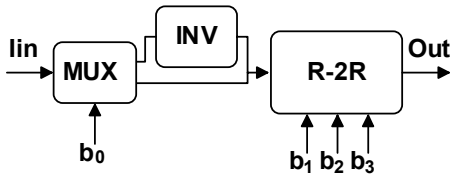

Figure 2: Block diagram of the multiplier structure

2.1.1 Programmable current divider

The main four-quadrant multiplier building block consists of an R-2R ladder circuit implemented with NMOS transistors. This structure (Fig. 3), widely presented in the literature [5] [6], allows the current to flow in both directions and is designed using identical 0.3 µm length and 10 µm width transistors working in triode mode.

Gate voltages b_i (Fig. 3) control the current flow to the right-side transistors (b_i=0 v) or the left-side transistor (b_i=3.3 v). For N bits, output current is described according to

$$I_{out_1} = I_0\left(\sum_{n=1}^{N}\frac{b_n}{2^n}\right) \quad (1)$$

$$I_{out_2} = I_0\left(\frac{1}{2^N}+\sum_{n=1}^{N}\frac{\bar{b}_n}{2^n}\right) \quad (2)$$

where I_{out1} and I_{out2} are the upper and lower output currents. In our work, I_{out1} has been selected as the final output current. Thus, according to (1), digital weight absolute value ranges from 0 to $1-1/2^N$. Assuming a 7 bits plus sign weight representation, digital operand minimum module value equals to $7.8125\cdot10^{-3}$.

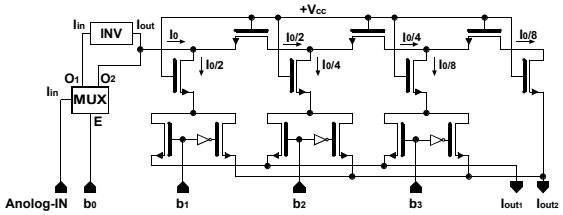

Figure 3: A 3-bit NMOS-based R-2R current ladder

2.1.2 Current inverter

Multiplier sign bit is implemented using a class AB current follower (Fig. 4). This structure gives a centered low-distortion current using a ± 2 v bias voltage. Tables 1 and 2 show the current follower design characteristics and transistor sizes, respectively. The bias current value (30 µA, see Table 1) ensures a very low distortion in the processing signals range. The resistor value in the middle of the structure is 66.66 kΩ.

2.2 Activation function

Activation function circuit consists of a class AB current conveyor (Fig. 5), similar to the circuit proposed in [7]. Circuit output has a hyperbolic tangent type behavior. Design characteristics and transistor dimensions are shown in Tables 3 and 4 respectively.

3 CIRCUIT SIMULATION

Artificial neuron circuit simulation was carried out using two different simulators (Spectre and Hspice) using Cadence Design Framework, obtaining similar results.

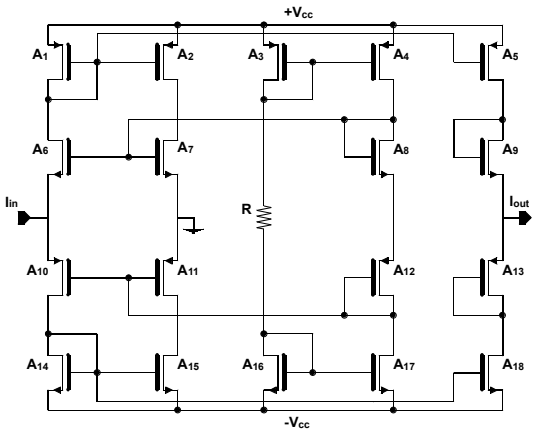

Figure 4: Current follower circuit

PARAMETER	VALUE
$\pm V_{cc}$ [V]	±2
I_{bias} [µA]	30
Vgs [V]	±1
Vds [V]	±1

Table 1: Current follower design characteristics

Transistors	W [µm]	L [µm]
A_1,A_2,A_3,A_4,A_5	4.25	0.3
A_6,A_7,A_8,A_9	13.00	0.3
$A_{10},A_{11},A_{12},A_{13}$	48.15	0.3
$A_{14},A_{15},A_{16},A_{17},A_{18}$	0.85	0.3

Table 2: Current follower transistors dimensions

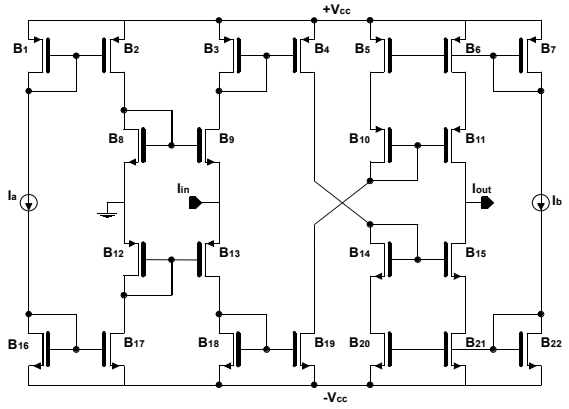

Figure 5: Class AB activation function

$\pm V_{cc}$ [V]	±2
I_a [µA]	5
I_b [µA]	50
V_{gs} [V]	±1
V_{ds} [V]	±1

Table 3: Activation function design characteristics

3.1 Mixed D/A four-quadrant multiplier

The mixed-mode multiplier behavior has been numerically modeled using Matlab. Realistic multiplier operation is expressed by:

$$c_{out} = 0.974865 w c_{in} - 0.0136726 c_{in} \quad (3)$$

Where c_{out} is the current output, w is the digital weight and c_{in} is the current input to the analog-digital multiplier. Fig. 6 presents the differences between the ideal and the real operation of the multiplier as a relative error:

$$err = 100 * (P' - P)/P \quad (4)$$

Transistors	W [µm]	L [µm]
B_1, B_2, B_3	0.9	0.3
B_4	5.35	0.3
B_5, B_6, B_7	6.9	0.3
B_8, B_9	1.9	0.3
B_{10}	2.85	0.3
B_{11}	0.65	0.3
B_{12}, B_{13}	8.7	0.3
B_{14}	0.7	0.3
B_{15}	0.6	2.1
B_{16}, B_{17}, B_{18}	0.6	1.7
B_{19}	1.2	0.3
B_{20}, B_{21}, B_{22}	1.4	0.3

Table 4: Activation function transistors dimensions

Where P' is the real multiplier operation and P is the ideal product. As it can be seen from (3), multiplier relative error is only dependent on the weight value.

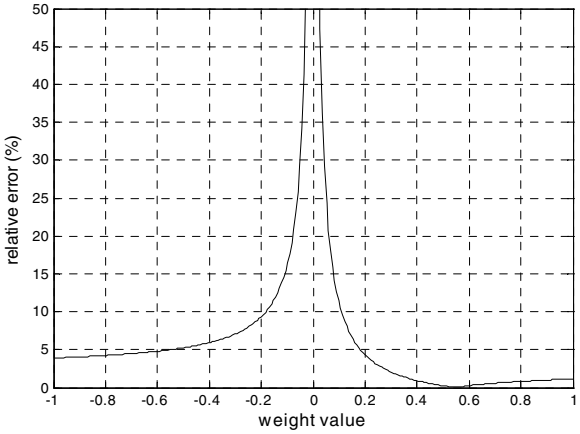

Figure 6: Ideal and real multiplier: Relative error

3.2 Non-linear activation function

Non-linear output function behavior has been modeled in Matlab using a look-up table. Simulated and ideal sigmoid function differences are presented in Figure 7. Higher error values close to the null current input are due to an offset that raises the whole circuit output.

4 EXAMPLE APPLICATIONS

In order to verify the proposed conditioning circuit performance, two sensor conditioning applications have been developed: The first one extends the limited linear behavior of two samples of negative temperature coefficient resistors with an error lower than 1 K; in the second application two samples of giant magneto-resistive sensors are linearized, achieving an error lower than 1 degree in angular

position measurement, doubling the sensor linear range.

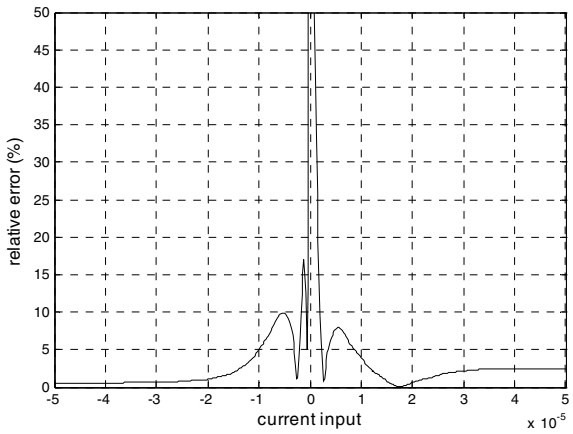

Figure 7: Implemented and ideal non-linear function: Relative error

4.1 Extending the linear range of an NTC

Our goal is to extend the limited linear range of an NTC, using the proposed adaptive processor as main building block. After training a network consisting of one input (the resistor output), one output (the linearized output) and two hidden nodes (which process the input data), results show a dramatic response improvement. Table 5 compares the error achieved using the proposed conditioning scheme applied to two different NTC samples compared to the original sensor errors. Errors hold lower than 1 K along the whole sensor span.

Sensor	Linear range	Extended range	%
NTC #1	274-308 K	252-323 K	108
NTC #2	274-308 K	252-323 K	108
GMR #1	252-305 deg	198-328 deg	145
GMR #2	234-292 deg	202-322 deg	107

Table 5: Range extensions for the sensor samples

4.2 Extending the linear range of a GMR

Similarly, an ANN with four nodes in the non-linear processing layer is trained in order to extend the limited linear range of a GMR angular sensor. As Table 5 shows, applying this solution to two different sensor samples, the achieved range extension is again significant. Last column in Table 5 shows the extended range as a percentage.

5 CONCLUSIONS

In this work we have presented the architecture and simulated behavior of a current-mode mixed digital-analogue processor built to extend the application range of a sensor, adapting the processing operation according to changes in the sensor behavior. Using the 0.35 μm Austria Microsystems design kit, the system process data in analogue current mode, storing the processing coefficients (weights) in digital technology, much better than analogue for long-term data storage. Moreover, modification of these parameters according to processing specifications is very easy, giving the expected performance. The application of this processor to conditioning several different sensor samples shows promising results. The limited power and size of analogue circuits make the proposed block suitable to be implemented in smart sensors.

Acknowledgments

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